REMARKS/ARGUMENTS

Claims 1-39, 42, 43, 45, 49-52, 54, 56, 58, 60 and 81 are pending in this application. All pending claims have been rejected. Claims 2-5, 8, 9, 15-18, 21 and 22 have been amended.

The drawings stand objected to as FIGS. 1, 2, 13, 14, and 20 do not show the "Prior Art" legend. Figures 1, 2, 13, 14, and 20 have been amended to include the label designation as suggested by the Examiner.

Claims 1-39, 42, 43, 45, 49-52, 54, 56, 58, 60 and 81 stand rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter of the invention. The rejection of the pending claims, as amended, under 35 USC 112, second paragraph, is respectfully traversed.

Regarding claim 81, the recitation of "a ferroelectric capacitor circuit ... coupled between the internal node of the first logic gate and the internal node of the second logic gate" is deemed to be neither indefinite nor misdescriptive. Figure 4 clearly shows a "ferroelectric capacitor circuit" including ferroelectric transistors z0, z1, z10 and z11. As noted by the Examiner, the ferroelectric capacitor circuit is coupled to the outputs "via the switches controlled by [the] WL and WLB signals". (Underlining Added). In the construction of claim 81, the "first logic gate" and the "second logic gate", each include one of the switches, along with other transistor elements. It is deemed clear that a "logic gate" can include a "switch", if desired, and there is no obligation to claim these elements separately. The "switch" is a part of the logic gate, one end of which forms the "internal circuit node" of the logic gate that is coupled to the ferroelectric capacitor circuit. For these reasons claim 81 is deemed to be allowable under 35 USC 112, second paragraph.

Regarding claims 2 and 3, these claims have been amended to remove the recitation of the "internal circuit node" and more clearly claim the invention as described and shown in the specification. No new matter has been added to claims 2 and 3. Claims 4-5 and 15-18 have been similarly amended. No new matter has been added to claims 4-5 and 15-18. It is deemed that claims 2-5 and 15-18, as

Amendments to the Drawings:

The attached sheets of drawings include the "Prior Art" legend to Figs. 1, 2, 13, 14, and 20. Annotated sheets showing changes are not believed necessary for these minor changes, but can be provided if required.

Attachment: Replacement Sheets

amended, are now sufficiently clear and therefore are allowable under 35 USC 112, second paragraph.

Regarding claims 8 and 9, these claims have been amended to also remove the recitation of the "internal nodes" and are now deemed to be sufficiently clear and allowable under 35 USC 112, second paragraph. Claims 21 and 22 have also been similarly amended. No new matter has been added to claims 8-9 and 21-22.

For the above reasons, all pending claims are deemed to be allowable under 35 USC 112, second paragraph.

Claims 81, 1, 10, 11, 12, 14, 23 and 24 stand rejected under 35 USC 102(b) as being anticipated by W0 01/15323 A1. The rejection of claims 81, 1, 10, 11, 12, 14, 23 and 24, as amended, is respectfully traversed. Claim 81 claims, in part, "a ferroelectric capacitor circuit including at least one ferroelectric load capacitor and at least one ferroelectric storage capacitor coupled between the internal node of the first logic gate and the internal node of the second logic gate". Figure 4 of W0 01/15323 A1 shows at least two differences when compared to the present invention, as claimed in claim 81. Firstly, one of the load or storage capacitors, as that term is used in the specification, is not a ferroelectric capacitor and thus a "ferroelectric capacitor circuit" as claimed is not taught. Secondly, the designated "ferroelectric capacitor circuit" is not coupled to the "internal nodes" of the first and second logic gates, but rather is coupled directly to the outputs of the gates. For these reasons, claim 81 is deemed to be allowable over the cited reference and allowable under 35 USC 102(b). The remaining claims are deemed to be allowable as being dependent upon an allowable base claim.

Claims 2-5 and 15-18 stand rejected under 35 USC 103(a) as being unpatentable over W0 01/15323 A1 in view of Applicant's cited prior art FIGS. 2 and 14. The rejection of claims 2-5 and 15-18 under 35 USC 103(a) is respectfully traversed. Claims 2-5 and 15-18 are deemed to be patentable as being dependent upon an allowable base claim.

Claims 27-31 and 35-37 stand rejected under 35 USC 103(a) as being unpatentable over Leuschner (US Patent No. 4,002,933) in view of W0 01/15323

A1. The rejection of claims 27-31 and 35-37 under 35 USC 103(a) is respectfully traversed. Claims 27-31 and 35-37 are deemed to be patentable as being dependent upon an allowable base claim.

The allowance of claims 6-9, 13, 19-22, 26, 32-24, 38-39, 42-43, 45, 49-52, 54, 56, 58 and 60 is acknowledged. However, it is deemed that in view of the foregoing remarks and amendments, that all claims are now sufficiently clear and are allowable over the cited references. The case is therefore deemed to be in condition for allowance, which is hereby respectfully requested.

No fee is believed due for this submittal. However, any fee deficiency associated with this submittal may be charged to Deposit Account No. 50-1123.

Respectfully submitted,

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